Roshan Samuel SoC Architect

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# Career Summary

23 years of experience as SOC, FPGA and Microcontroller Architect and Team Lead. 7 years of experience as designer with Verilog and PERL scripting. 17 patents issued, 1 pending. Wrote detailed micro-architecture specifications from marketing documents, including executive summary, design implementation, software interface, state machine diagrams, control flow charts and register bit descriptions. Trained and shepherded Design Engineers all the way to device tape-out.

# Expertise

Ability to translate rough or vague ideas into detailed, designable specifications. People skills to present ideas to a wide audience and gain consensus. Trainer and Mentor to junior Engineers.

# Technical Skills

Verilog, C, PERL, architecture expertise in ADC-based touch interfaces, I2C, SPI, FPGA fabric, AXI bus interface, embedded regulators, UARTs and programmable CRC calculators. Able to pull together a full-chip architecture document.

# Professional Experience

## FPGA Architect | Microchip Technology Inc. | Chandler, AZ Mar 2023 – Mar 2025

Architect for ultra low-end FPGA

* Gathered requirements from Marketing and built trackable requirements spreadsheet for ISO26262 compliance
* Explored AEC-Q100 and its relationship to Microchip Inc’s automotive certification process.
* Wrote preliminary Architecture Proposal document for review by management
* Wrote detailed Architecture document for Flash Controller
* Calculated bandwidth, memory sizes and implementation details for the various paths inside the device

## 8 and 16-bit Microcontroller Architect| Microchip Technology Inc | Chandler, AZ Mar 2003 – Mar 2023

Architect for PIC16, PIC18 and PIC24 Microcontrollers

* Architected PIC “Touchsense” capacitive touch controller using ADC capacitive charge-sharing
* Architected, from basics, a CPLD peripheral for PIC16 MCU. Currently marketed as the ‘CLB’ by Microchip.
* Architected, from basics, Microcontroller peripherals such as I2C, I2S, SPI, UART with full automation, LCD Graphics drivers, programmable CRC calculators, PWMs, dual-boot Flash systems, and full-chip architecture
* Trained Applications, Design, Software, Marketing and Product Engineers to bring the device to production

## Digital Designer | Texas Instruments | Dallas, TX Dec 1995 – Mar 2003

I wrote Verilog RTL for DSL Broadband chips. Also Architected and wrote RTL for digital audio chipset

* Wrote Verilog Code for FIFO management, PHY interfaces and Flash Controllers, managing clock crossings to prevent metastability
* Wrote PERL scripts to parse Verilog model output and automate test flows
* Used SignalScan to visually debug code

# Education

## Master’s Degree | Computer Science | Syracuse University 1994 – 1995

## Bachelor’s Degree | Electronics and telecommunications Engineering | Manipal Institute of Technology 1989 – 1993

# Interests

Toastmasters VP-Public Relations | Reef Aquarium Hobbyist